Docket No.: L&L-I0217

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : JÖRG BERTHOLD ET AL.

Filed : CONCURRENTLY HEREWITH

Title : METHOD FOR DETERMINING THE CRITICAL PATH OF AN INTEGRATED CIRCUIT

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

German Published Non-Prosecuted Patent Application DE 199 00 974 A1 (Matsumoto et al.), dated September 16, 1999, and English abstract thereof;

European Patent Specification EP 0 259 705 B1 (Hooper), dated March 16, 1988;

PCT WO 93/18468 (Misheloff), dated September 16, 1993;

Bowman, K. A. et al.: "Impact of Extrinsic and Intrinsic Parameter Fluctuations on CMOS Circuit Performance", IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, August 2000, pp. 1186-1193;

Eisele, M. et al.: "The Impact of Intra-Die Device Parameter Variations on Path Delays and on the Design for Yield of Low Voltage Digital Circuits", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 5, No. 4, December 1997, pp. 360-368;

International Search Report, dated June 24, 2003.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

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For Applicants

Date: July 15, 2003

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FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: L&L-I0217 Appl. No.: Applicant: JÖRG BERTHOLD ET AL. Filing Date: July 15, 2003 Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	199 00 974 A1	9/16/99	Germany				
	K	0 259 705 B1	3/16/88	Europe				
	L	93/18468	9/16/93	WIPO				
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Bowman, K. A. et al.: "Impact of Extrinsic and Intrinsic Parameter Fluctuations on CMOS Circuit Performance", IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, August 2000, pp. 1186-1193
		Eisele, M. et al.: "The Impact of Intra-Die Device Parameter Variations on Path Delays and on the Design for Yield of Low Voltage Digital Circuits", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 5, No. 4, December 1997, pp. 360-368

EXAMINER	DATE CONSIDERED